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**NORTH SOUTH UNIVERSITY**

**Department of Electrical and Computer**

**Engineering**

**Digital Logic Design (CSE 231)**

Faculty – Dr Mohammad Monirujjaman Khan(KMM)

Section: 06

Group: 04

**Project Part 2**

Circuit Diagram using Logisim

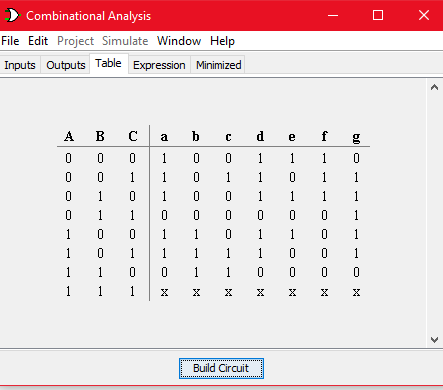
(­­Sop, Pos. Nand, Nor)

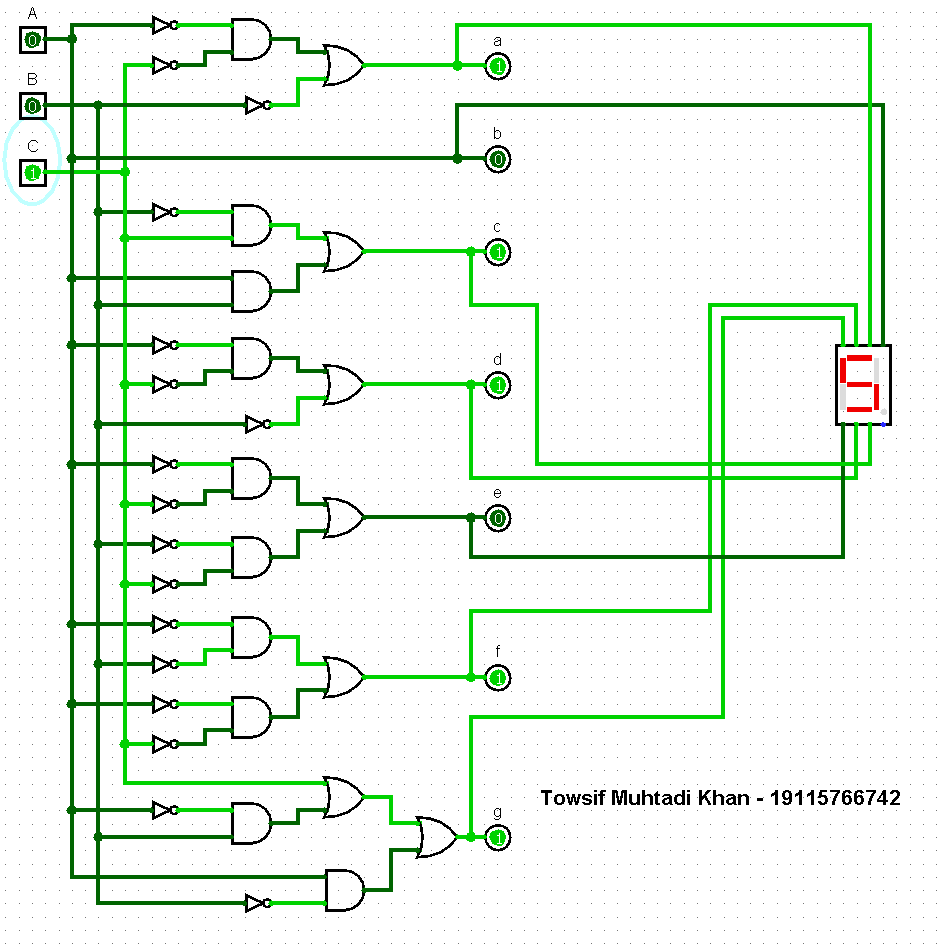
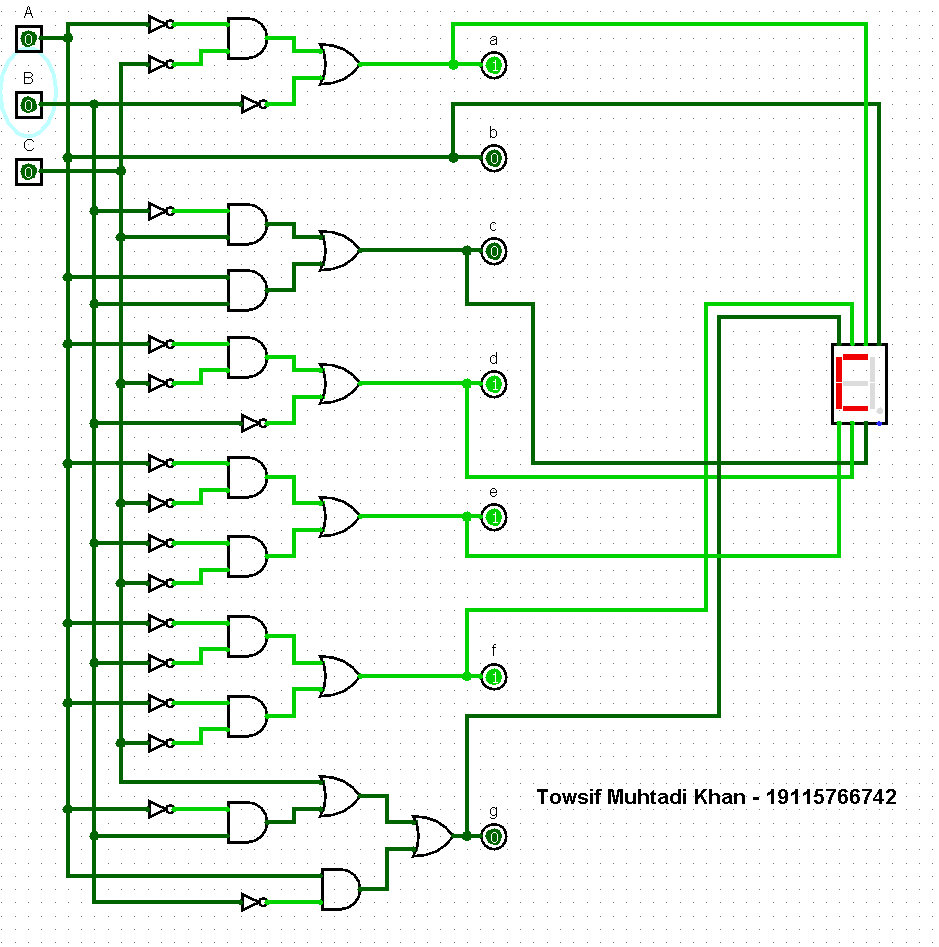
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| --- | --- |
| **Name** | **ID** |
| Towsif Muhtadi Khan | 1911576642 |
| Khalid Bin Shafiq | 1911342642 |
| Rafidul Islam | 1912152642 |
| Rashiqur Rahman Rifat | 1911445652 |

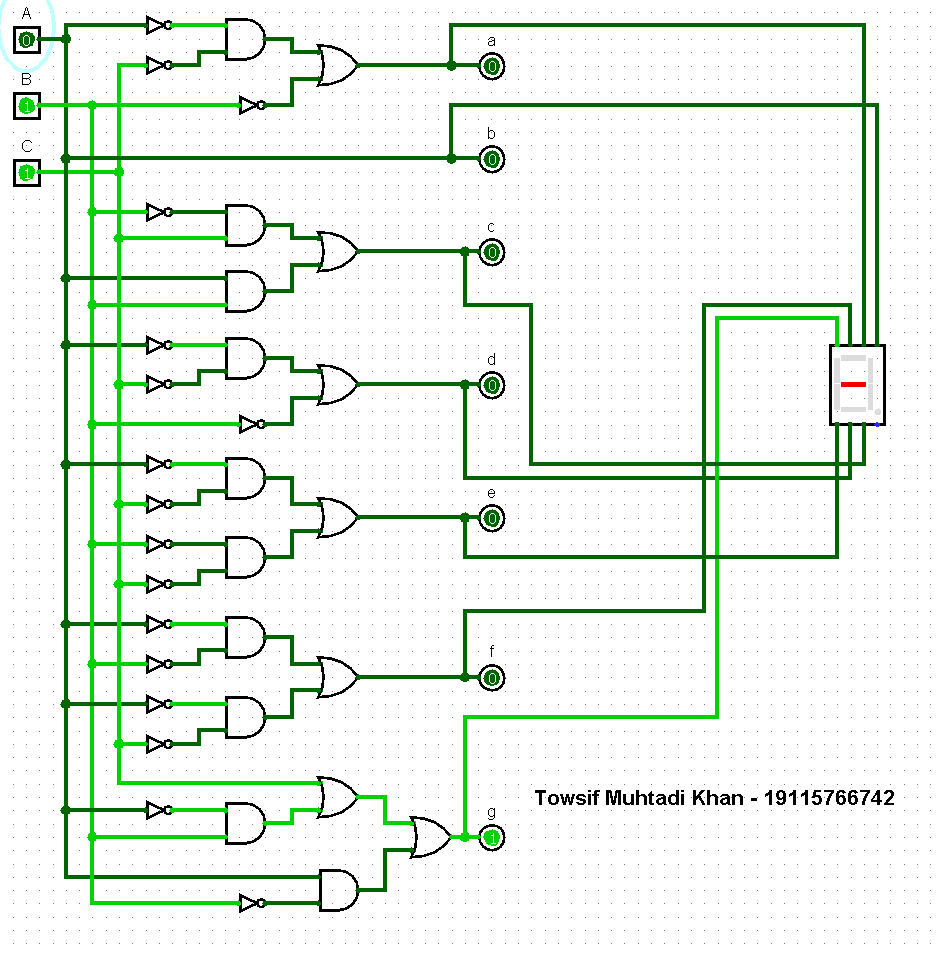
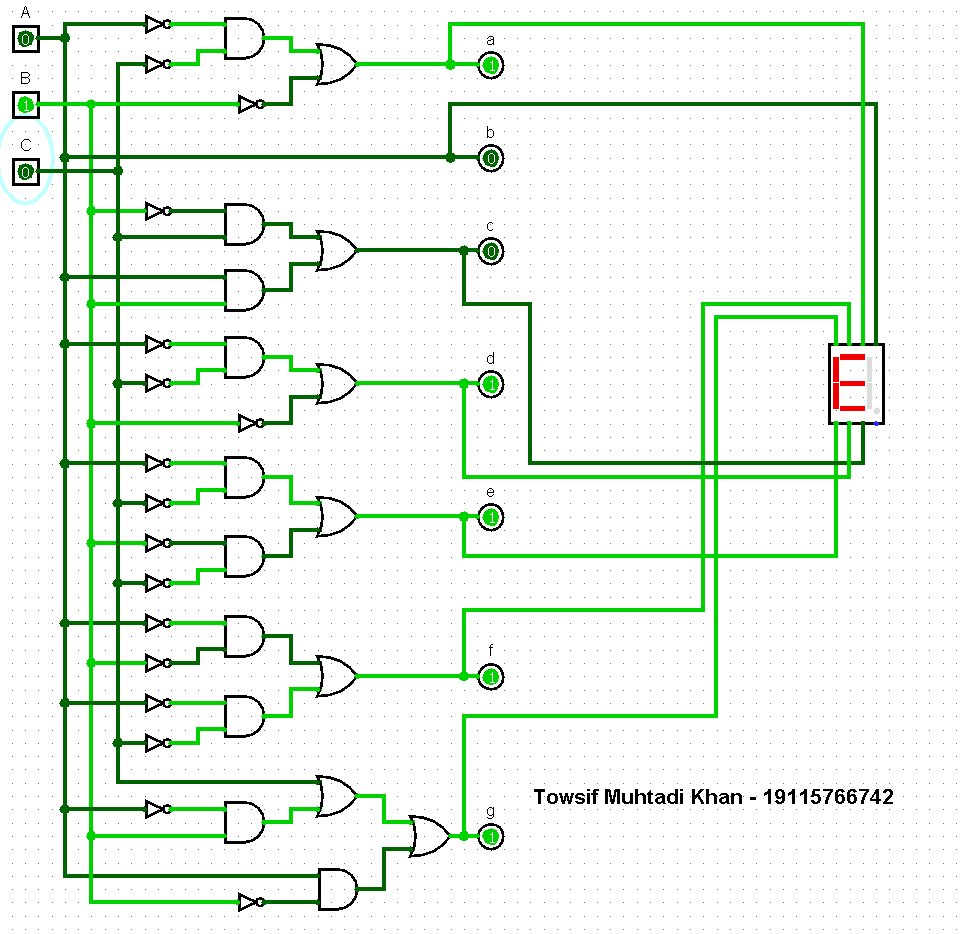
**CONTRIBUTION**

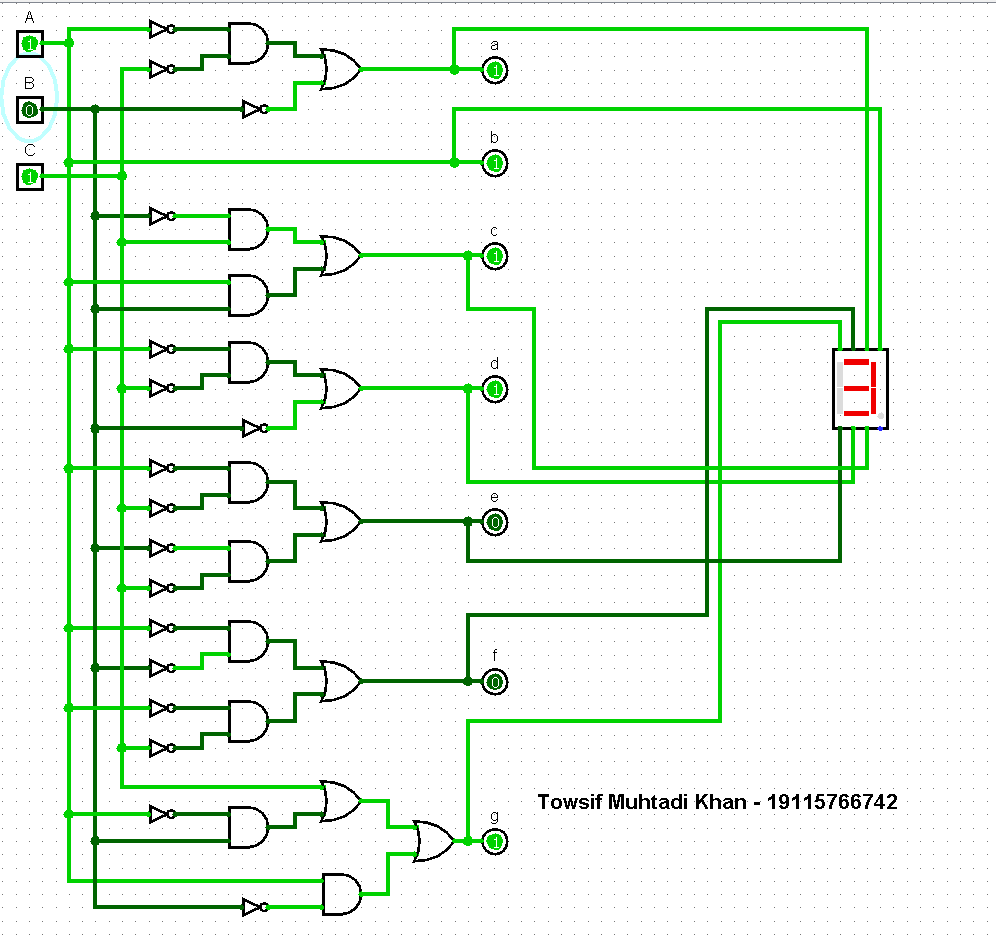
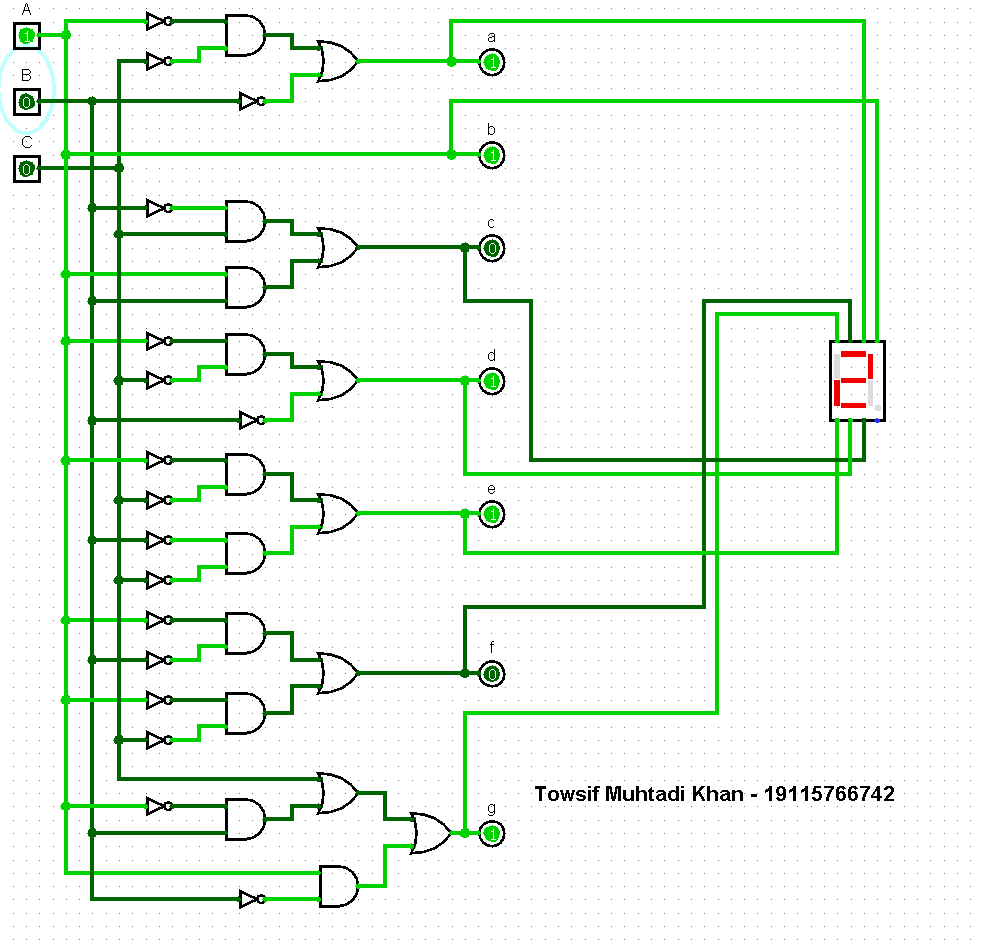
|  |  |
| --- | --- |
| Work done By | Topic |
| Towsif Muhtadi Khan  (Coordinator) | 1.Truth Table **(CSE-231)** |
| Rafidul Islam | 2. Circuit Diagram **(SOP)** |
| Rasiqur Rahman Rifat | 3. Circuit Diagram**(POS)** |
| Khalid Bin Shafiq | 6.Circuit diagram **(NAND Gate)** |
| Towsif Muhtadi Khan | 7.Circuit diagram **(NOR Gate)** |

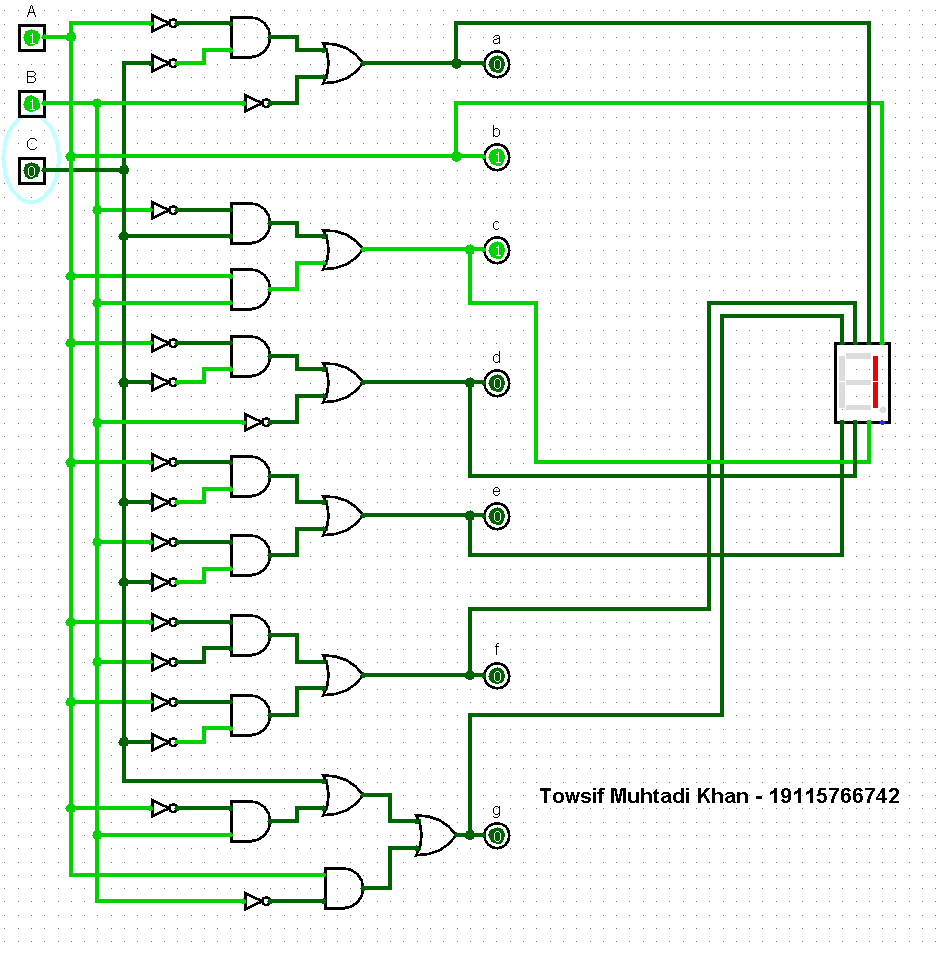
**Circuit from Truth table:**



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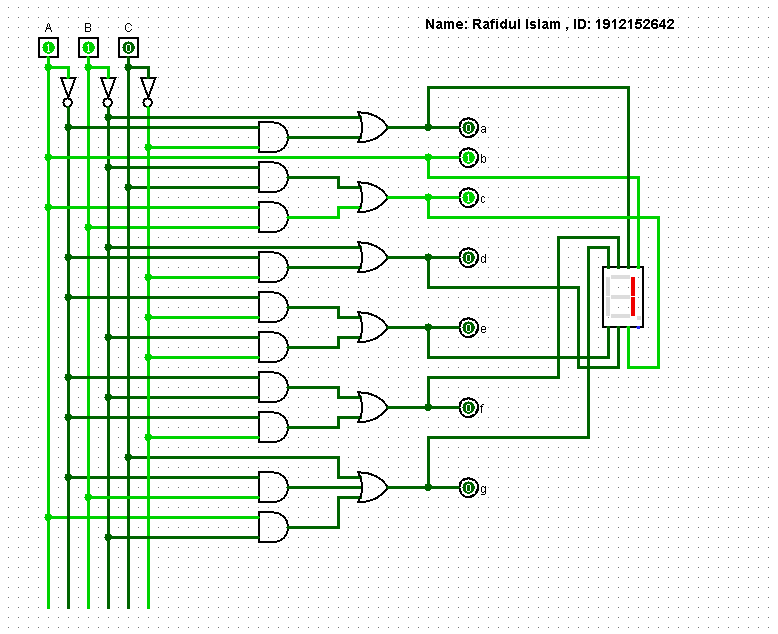
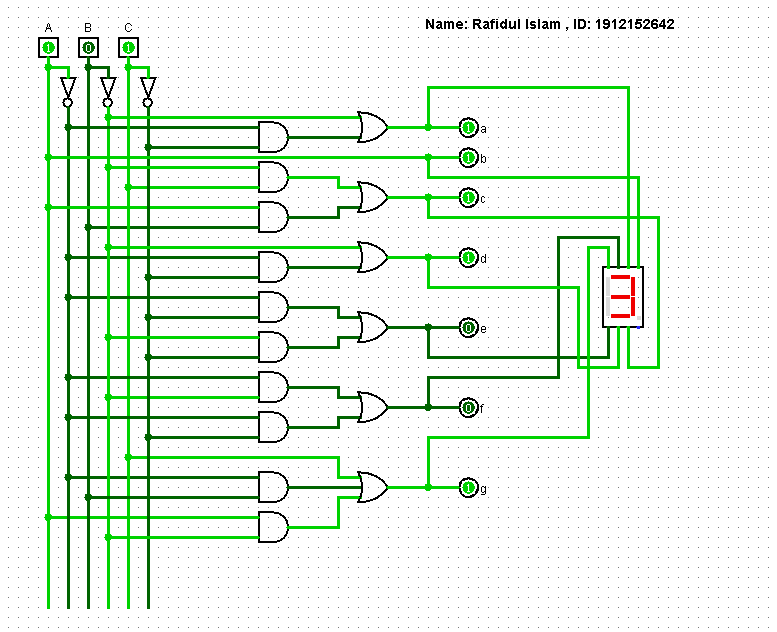
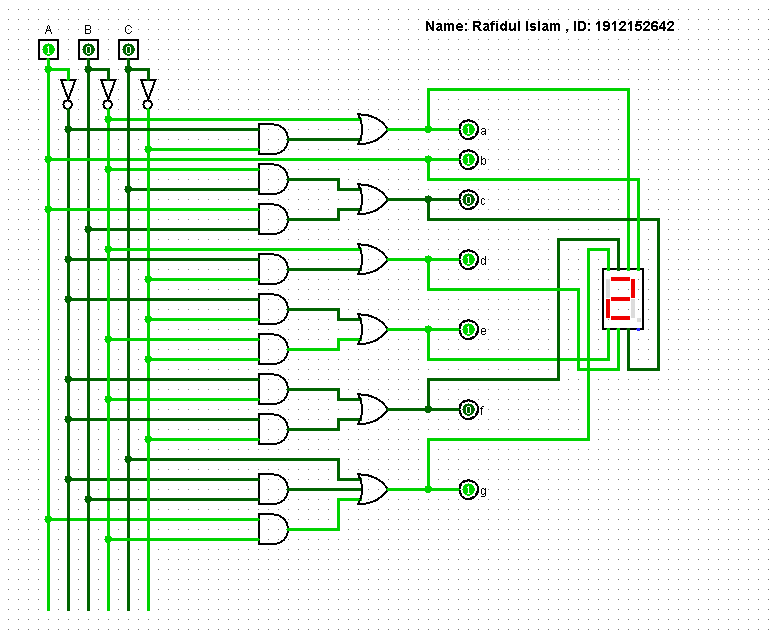
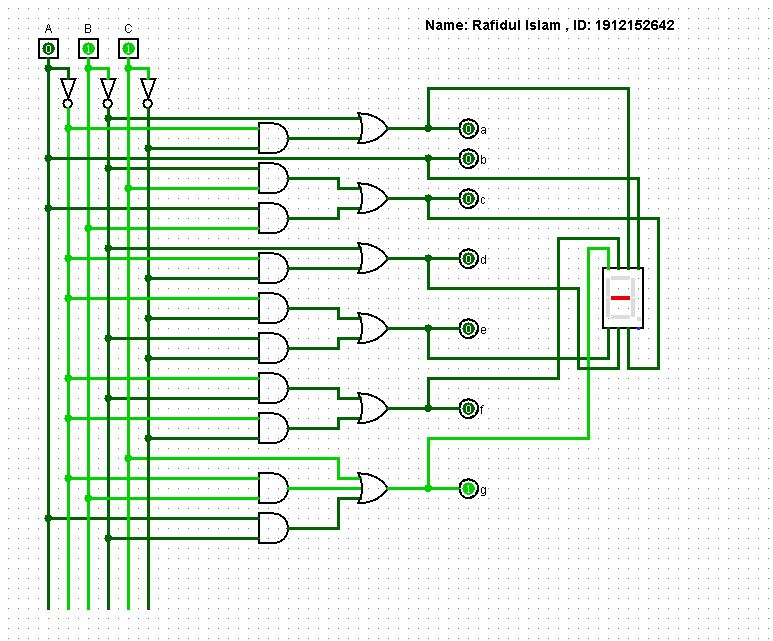
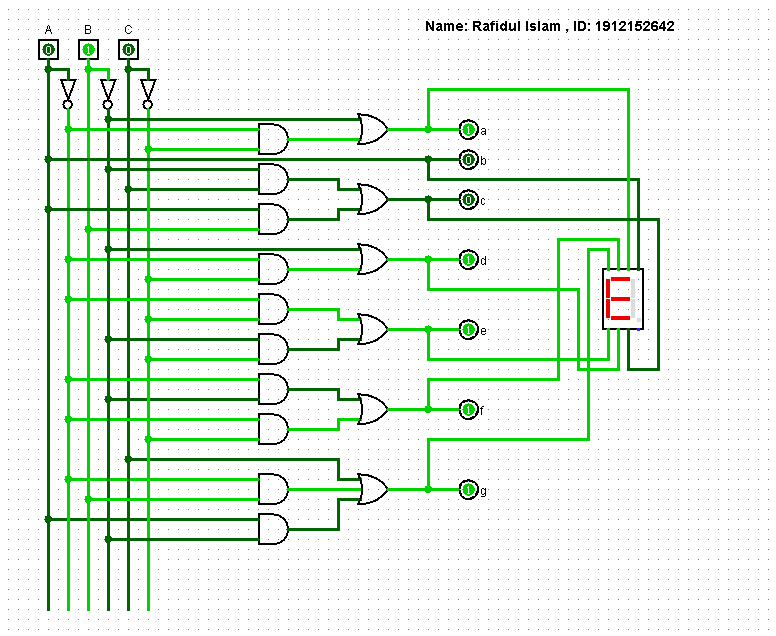
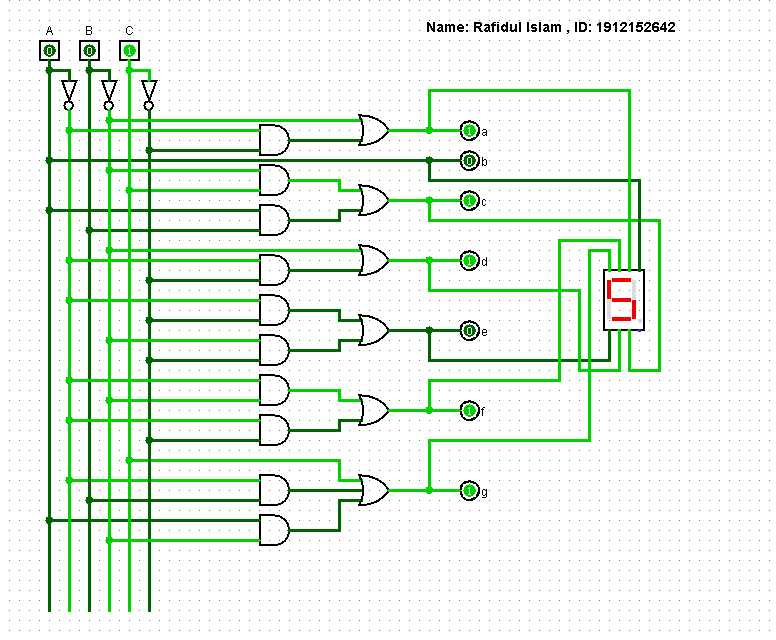
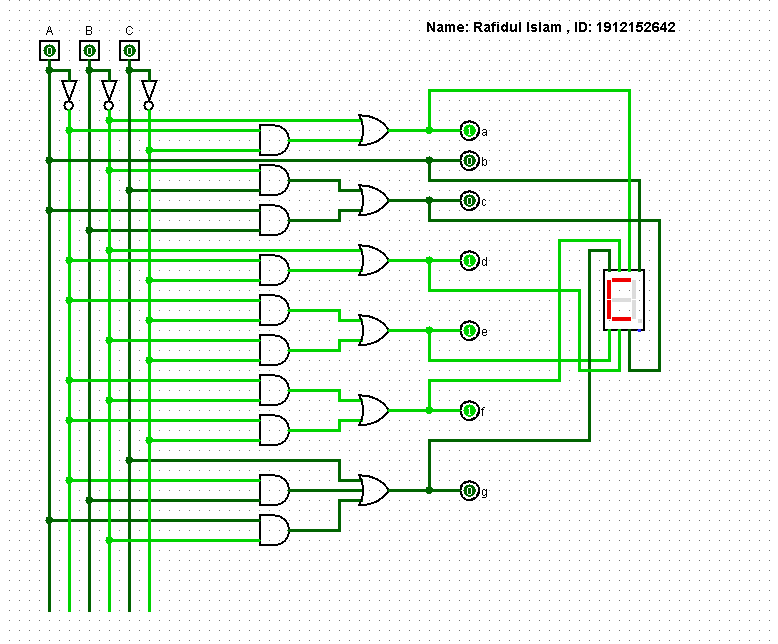
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Circuit diagram **(SOP)**

Applying SOP we got the following equations:

**a** = B’+A’C’, **b** = A, **c** = B’C+AB, **d** = B’+A’C’, **e** = A’C’ + B’C’

**f** = A’B’ + A’C’, **g** = C+A’B+AB’

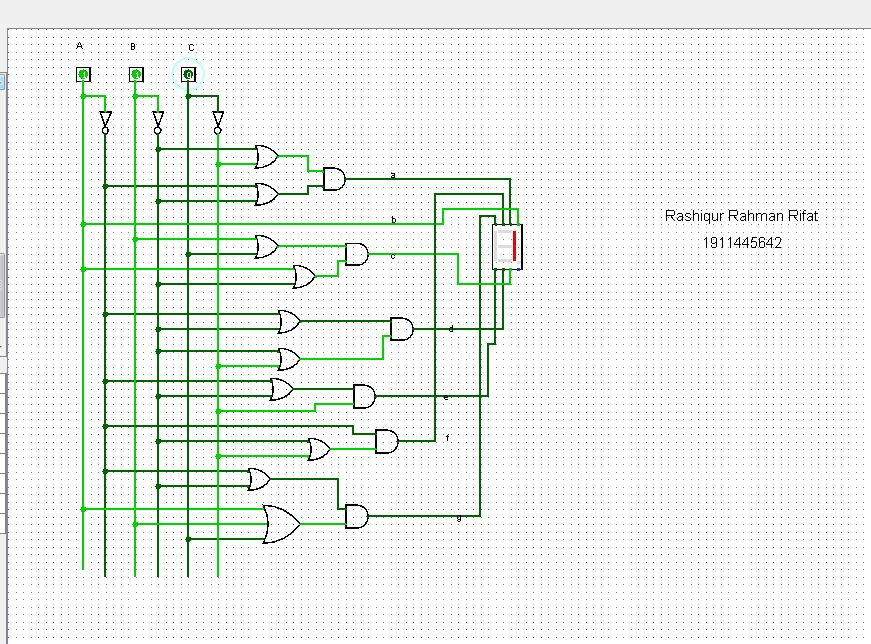
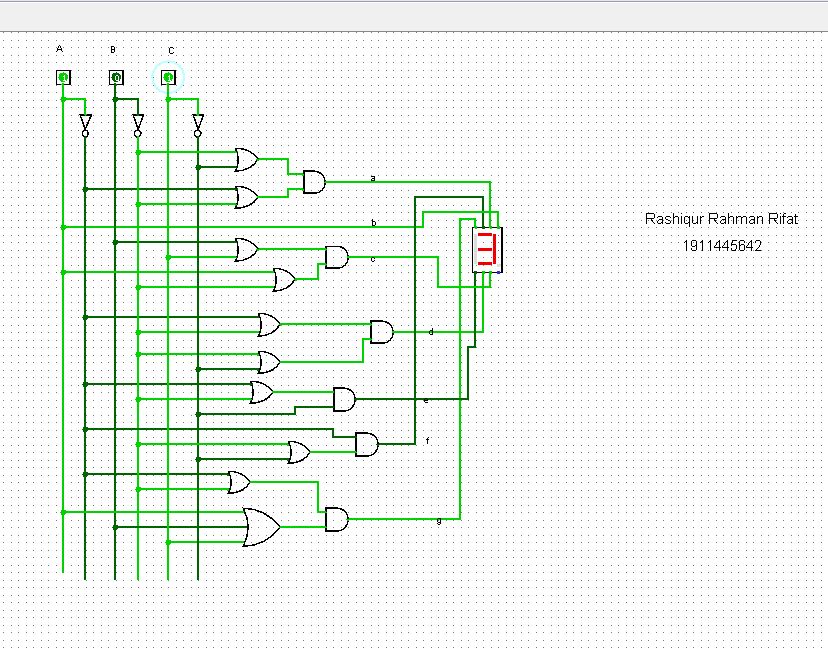
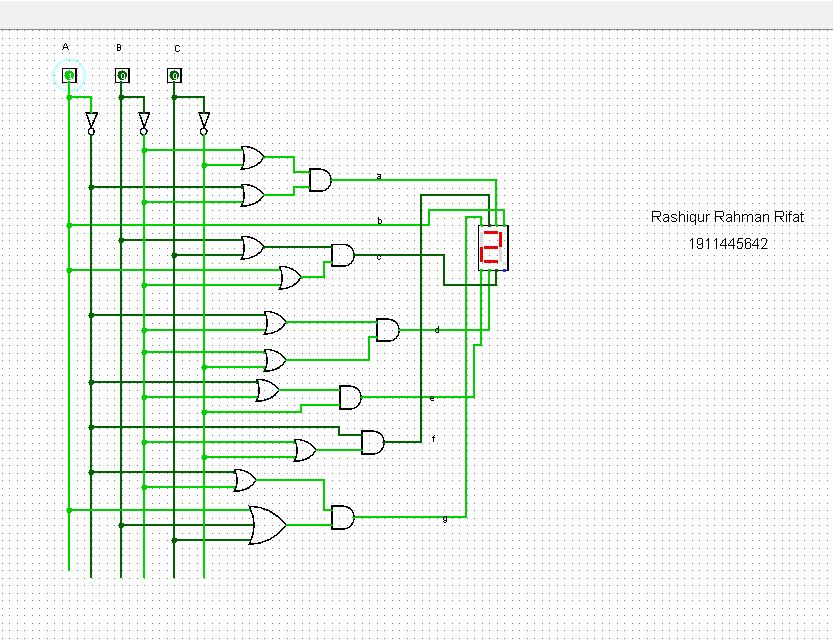
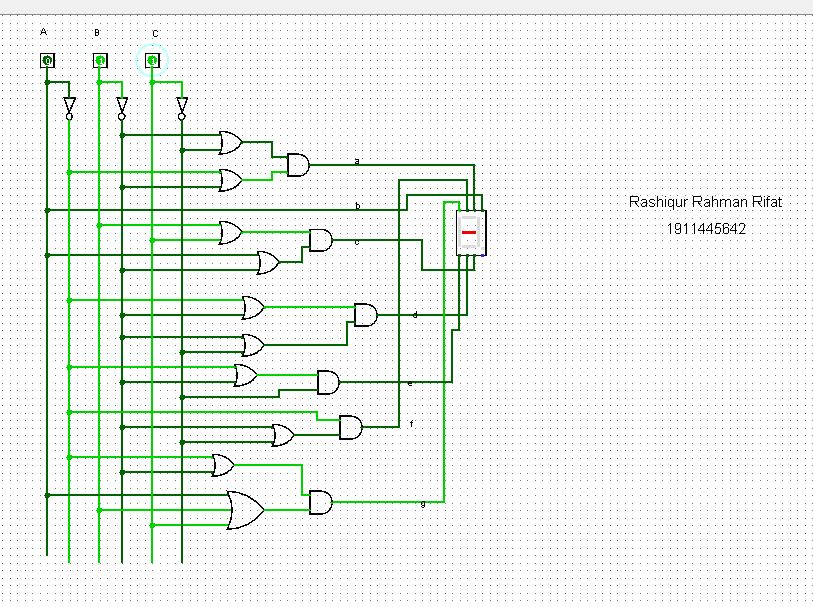
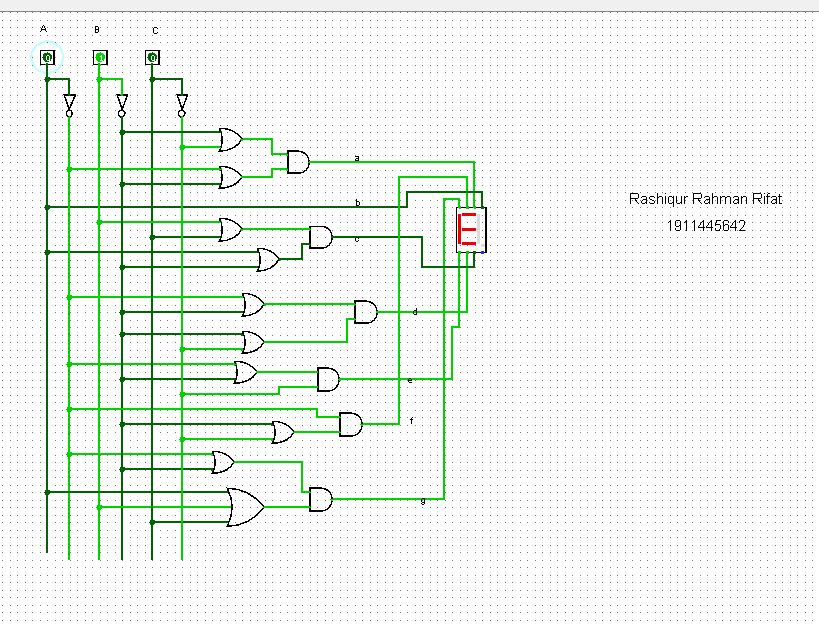
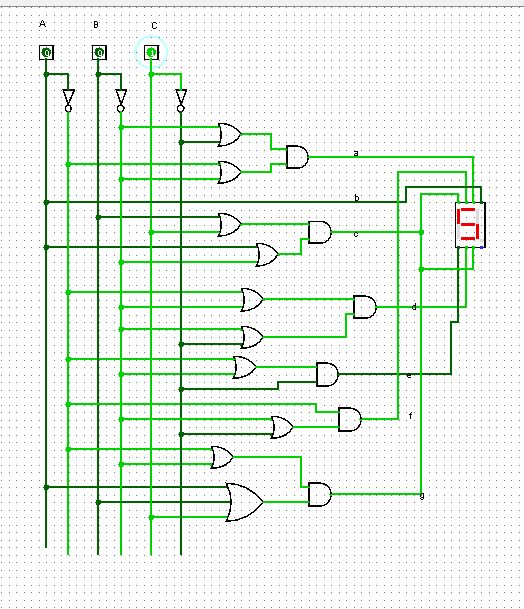
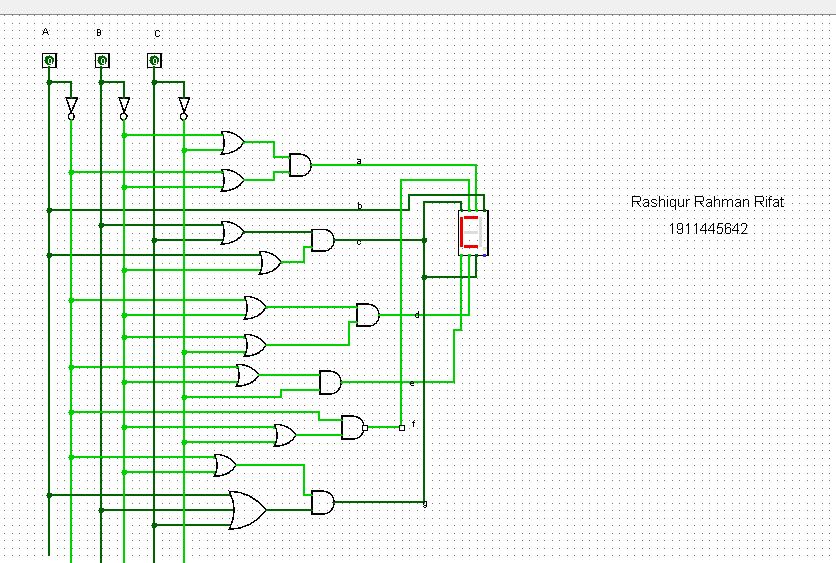


**Figure***: Circuit diagram* ***(SOP)***

Circuit diagram **(POS)**

Applying POS we got the following equations:

**a** = (B’+C’), **b** = A, **c** = (B+C) (A+B’), **d** = (A’+B’)(B’+C’), **e** = (A’+B’)C’, **f** = A’(B’ +C), **g** = (A’+B’) (A+B+C)



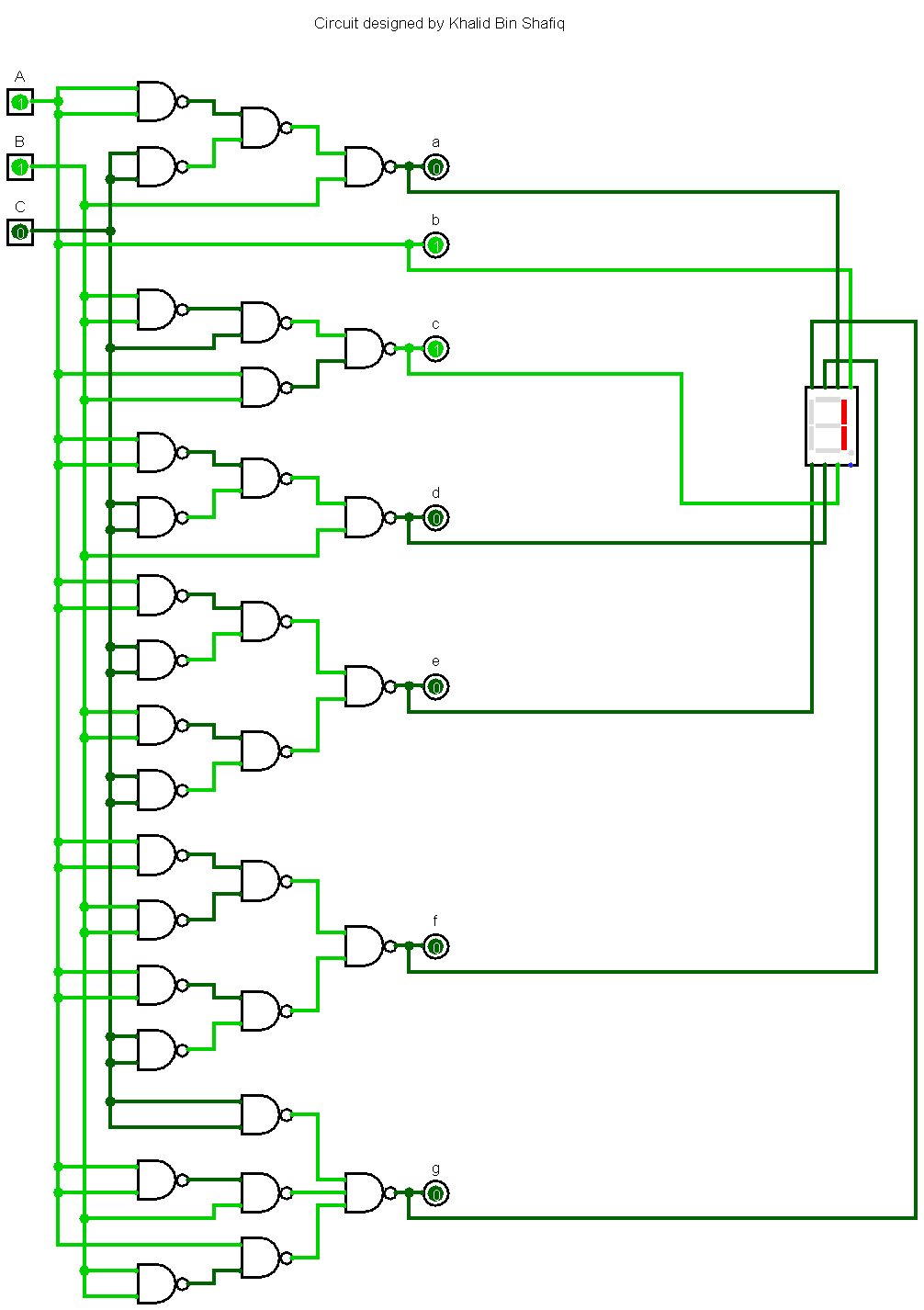
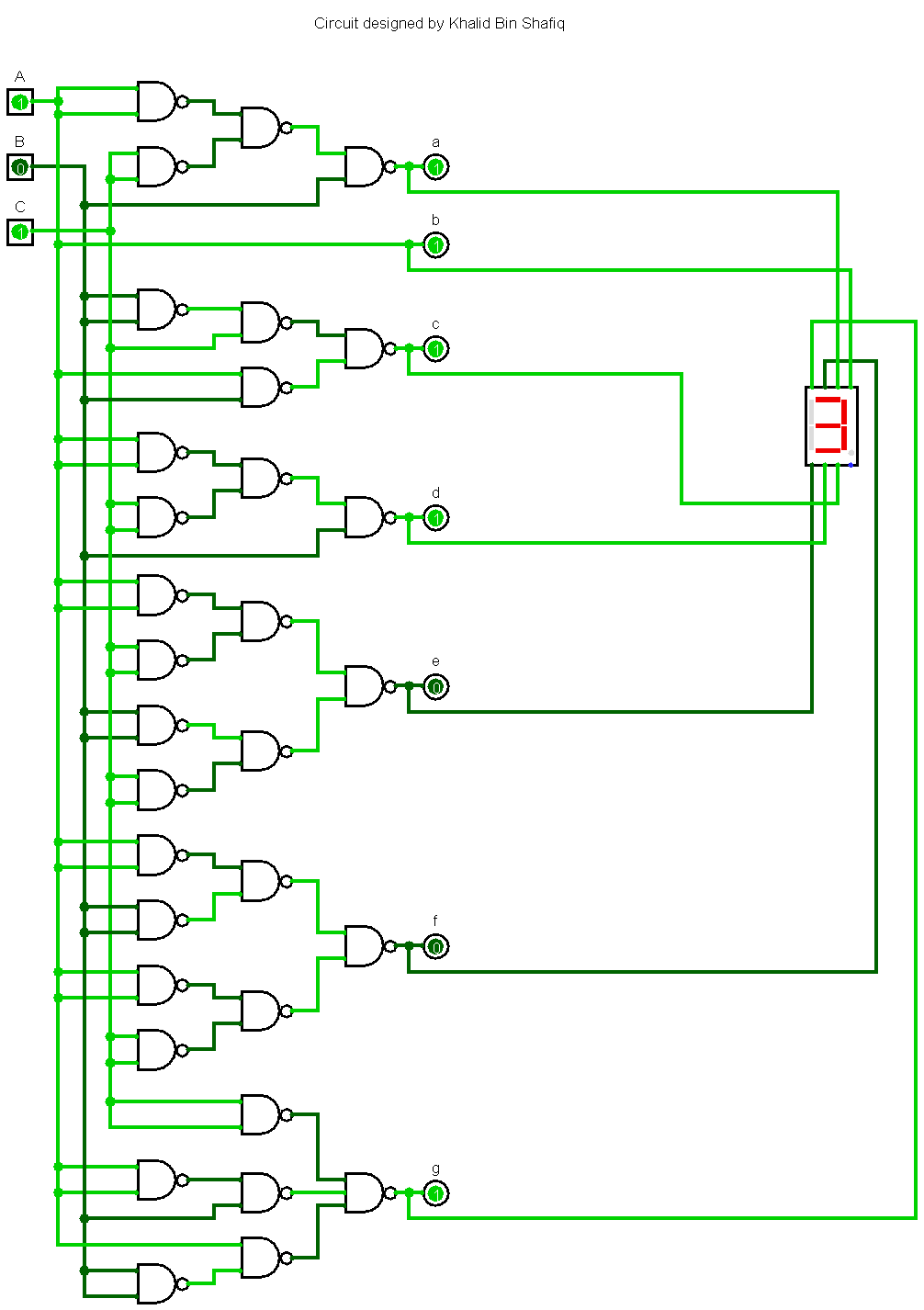
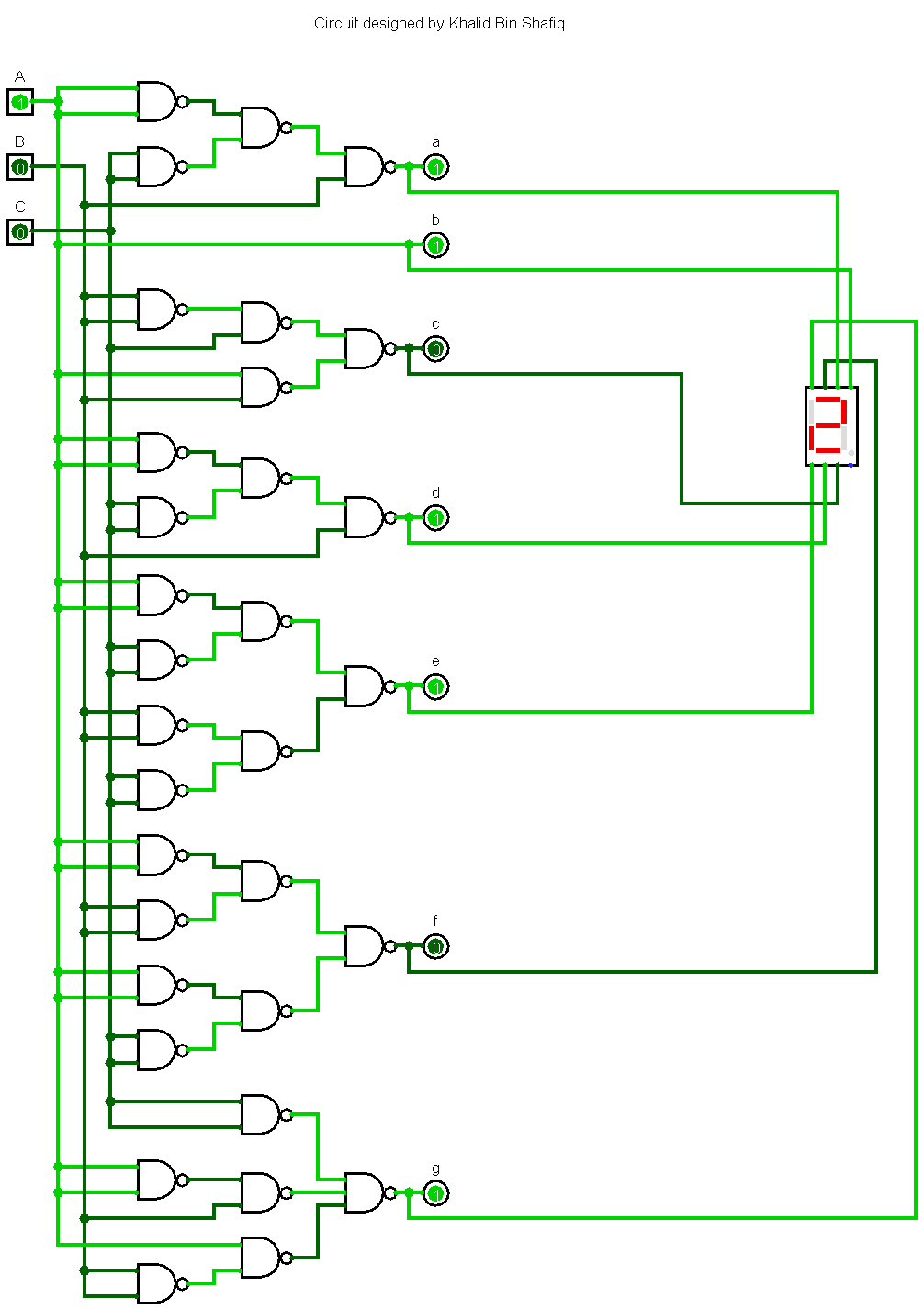
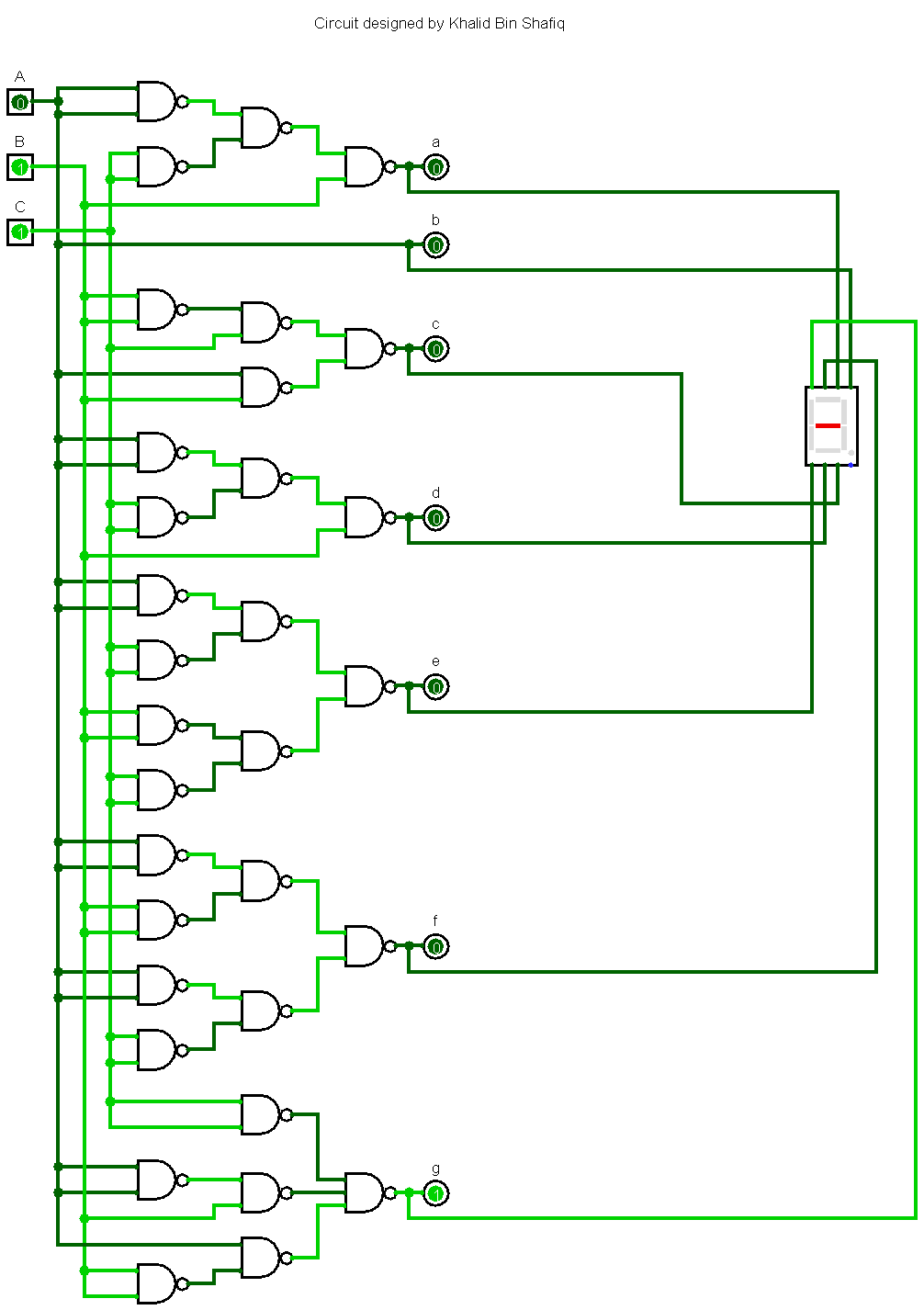
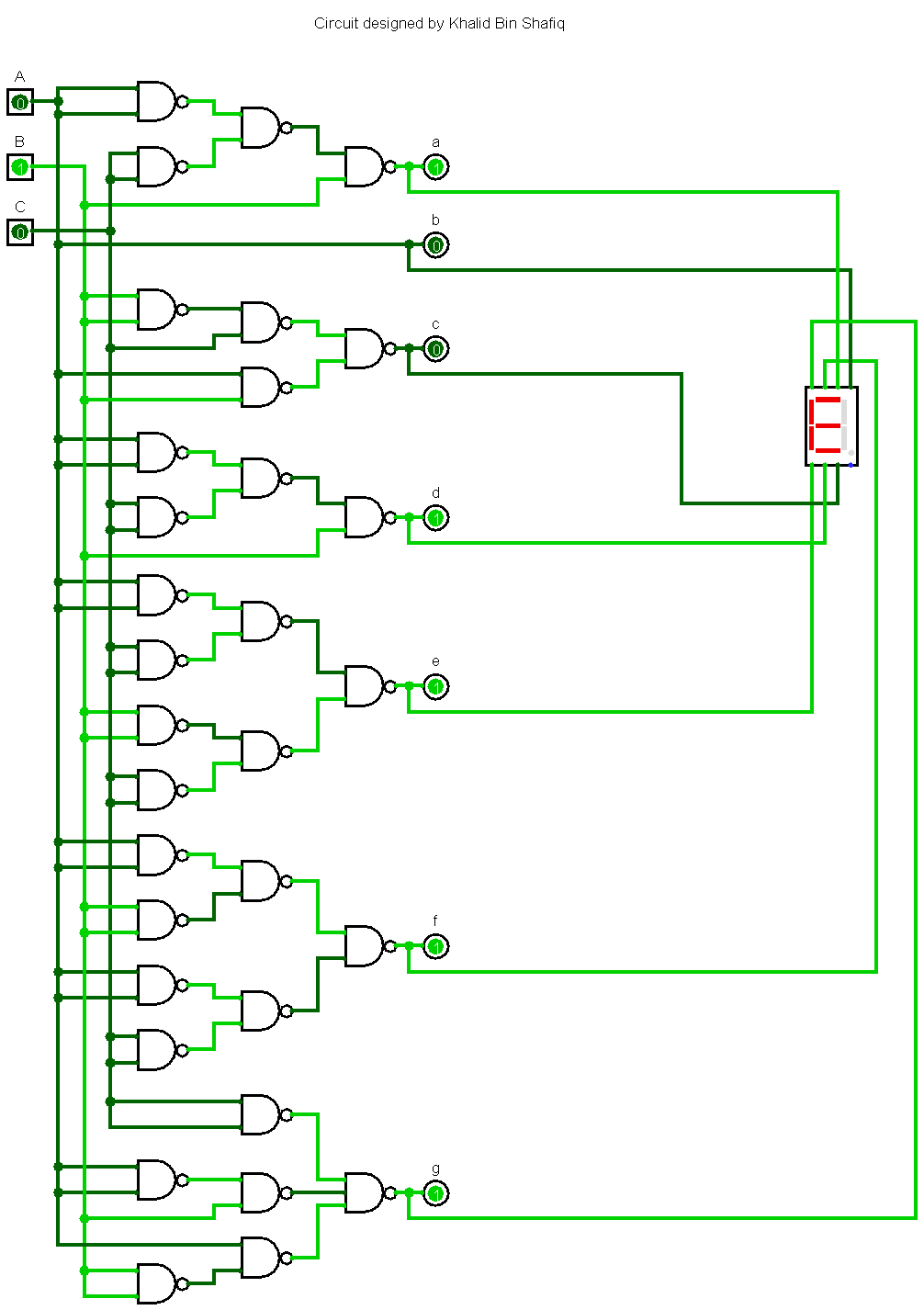
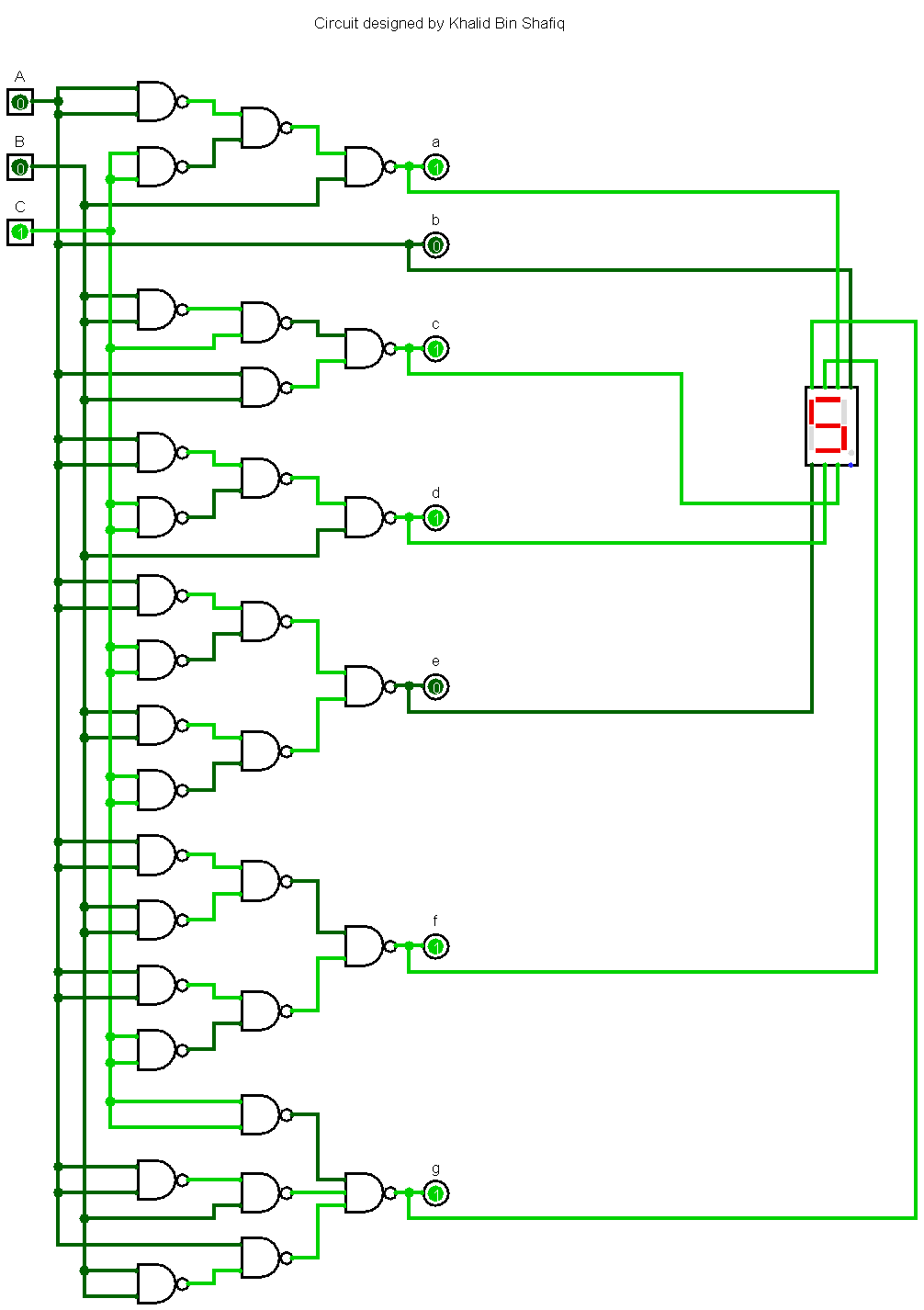
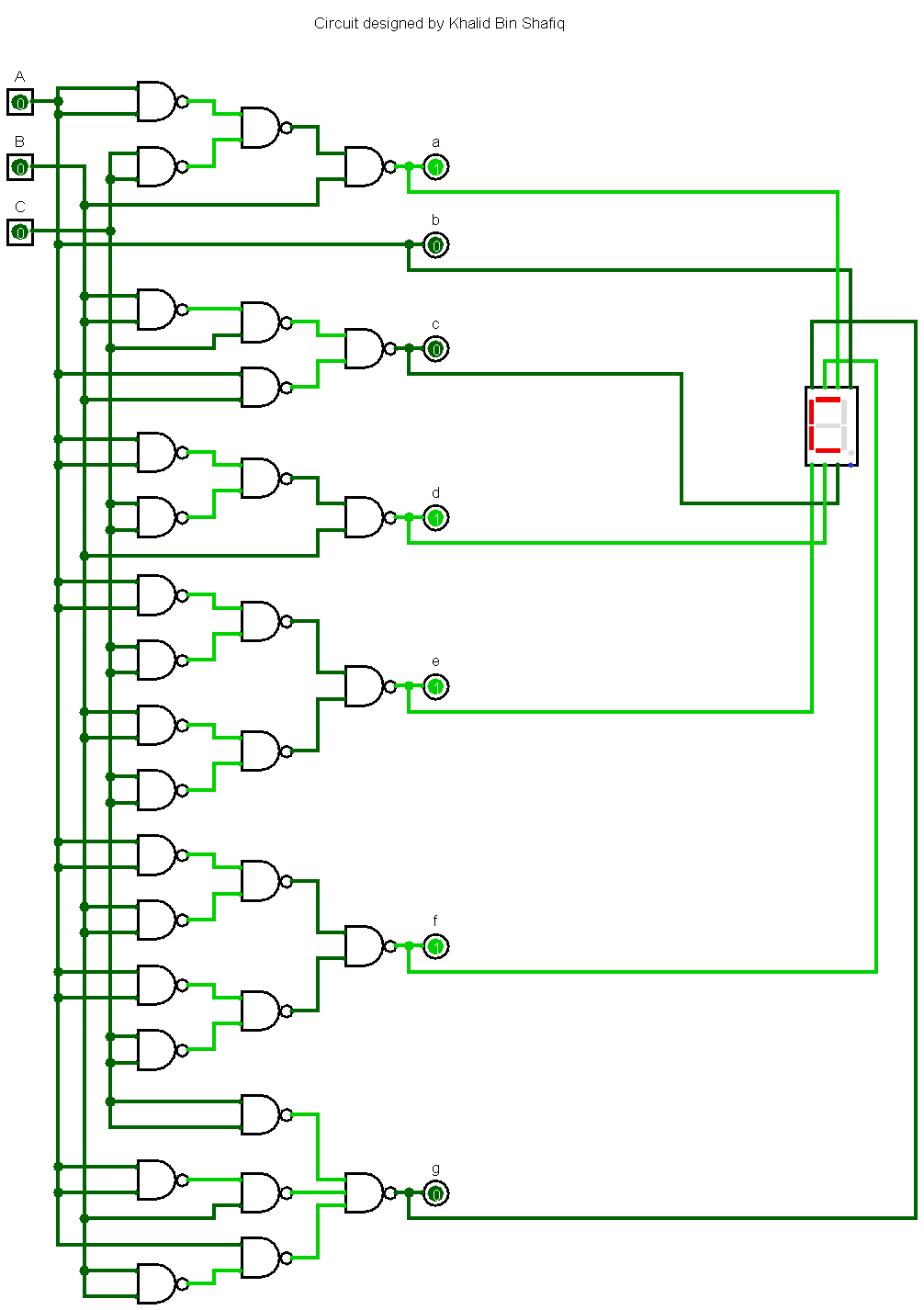
**Figure***: Circuit diagram* ***(POS)***

Circuit diagram **(NAND Gate)**

**a** = B’+A’C’, **b** = A, **c** = B’C+AB, **d** = B’+A’C’, **e** = A’C’ + B’C’

**f** = A’B’ + A’C’, **g** = C+A’B+AB’

The circuit diagram using NAND gates will be:



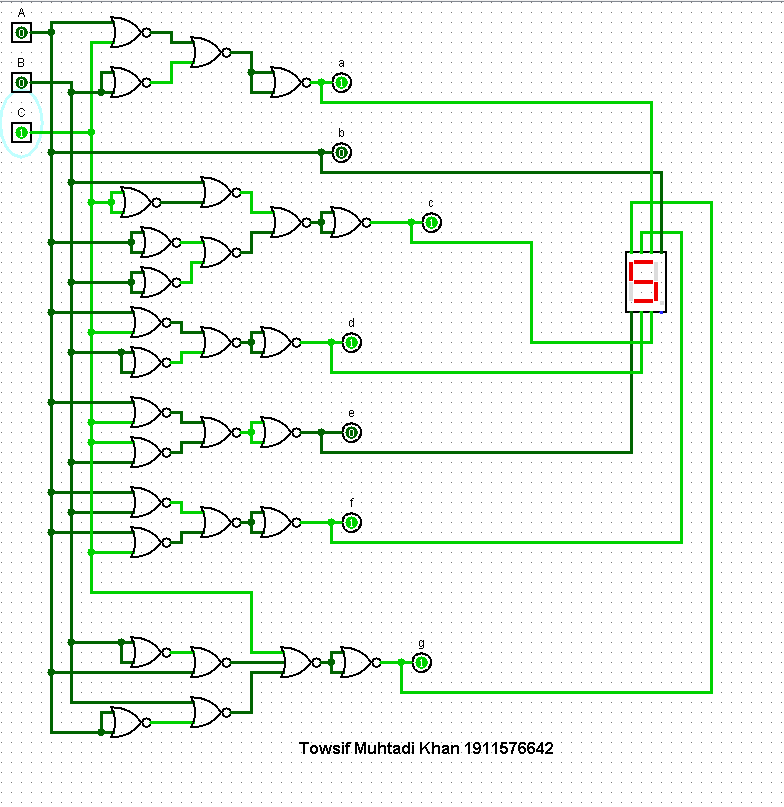
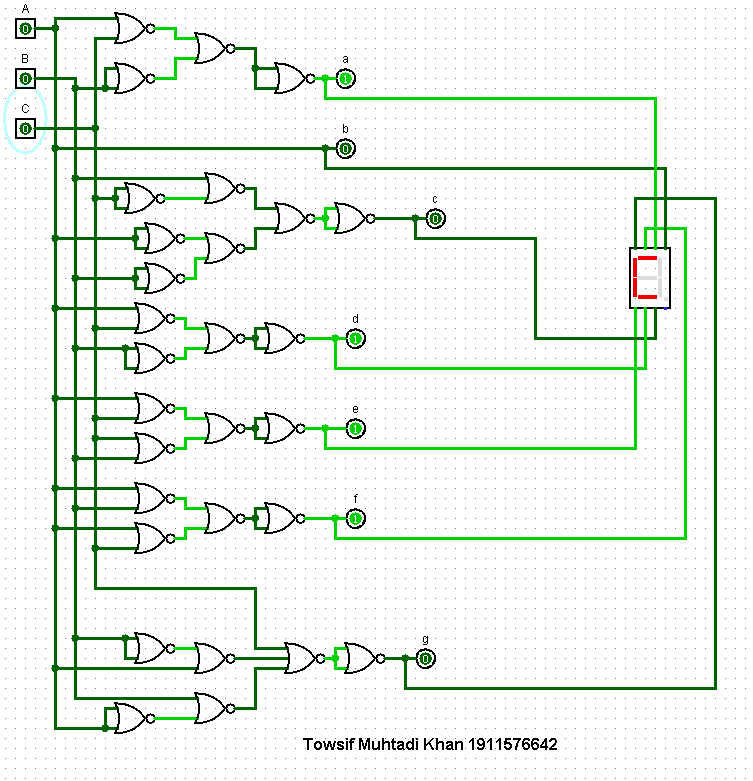
**Figure***: Circuit diagram* ***(NAND GATE)***

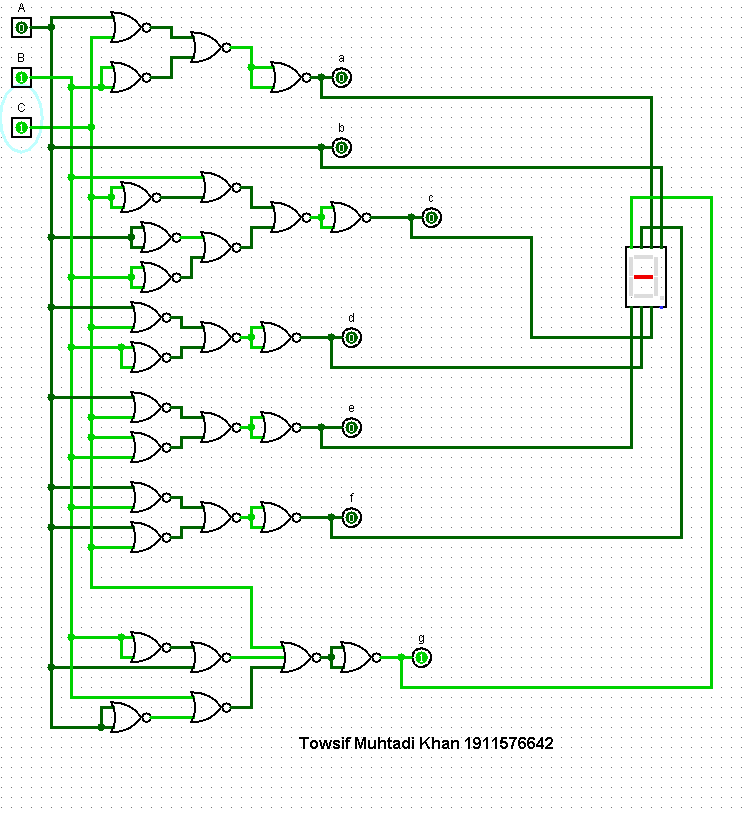
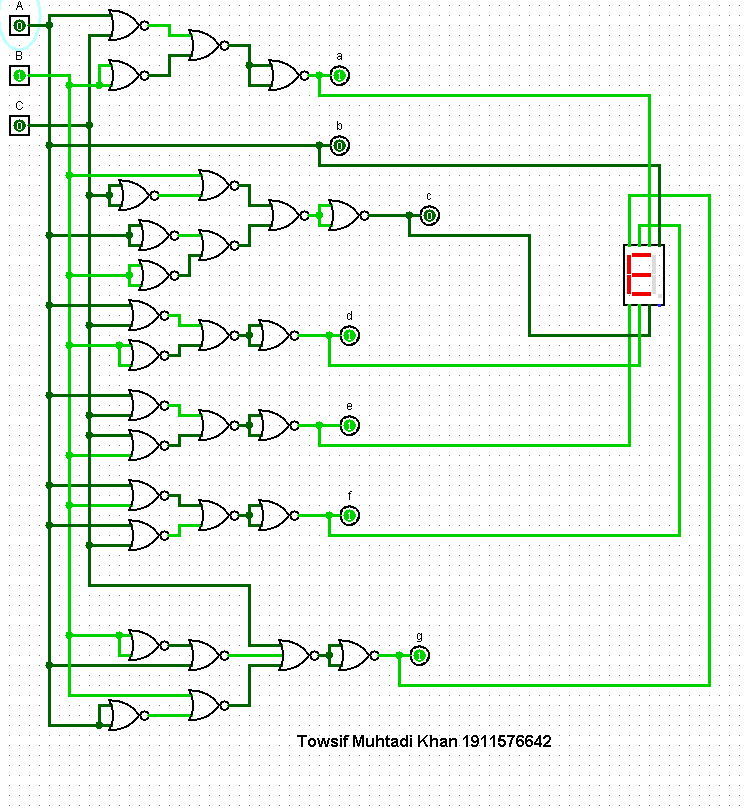
Circuit diagram **(NOR Gate)**

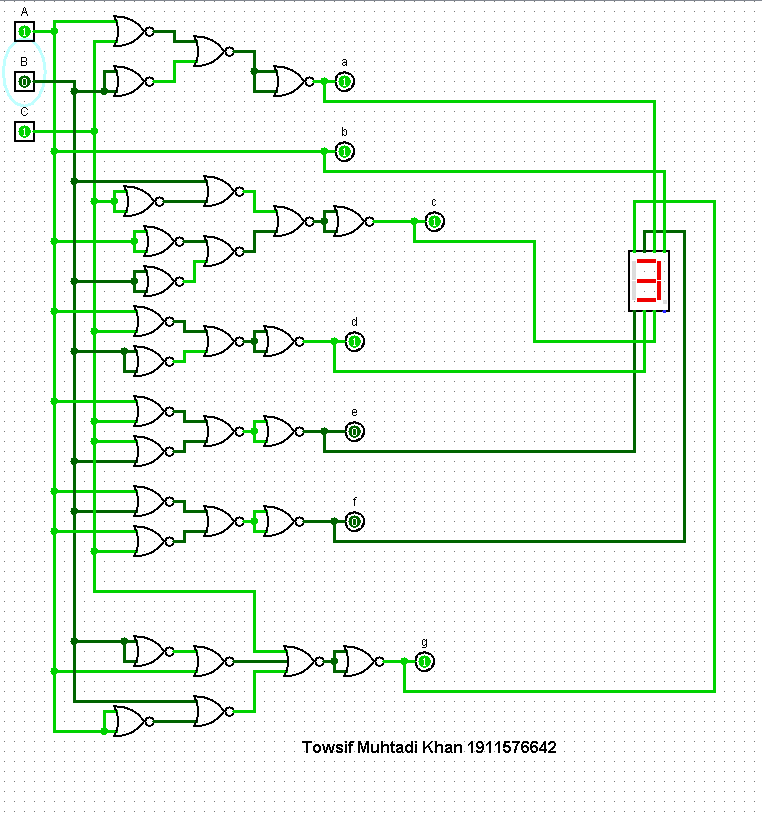
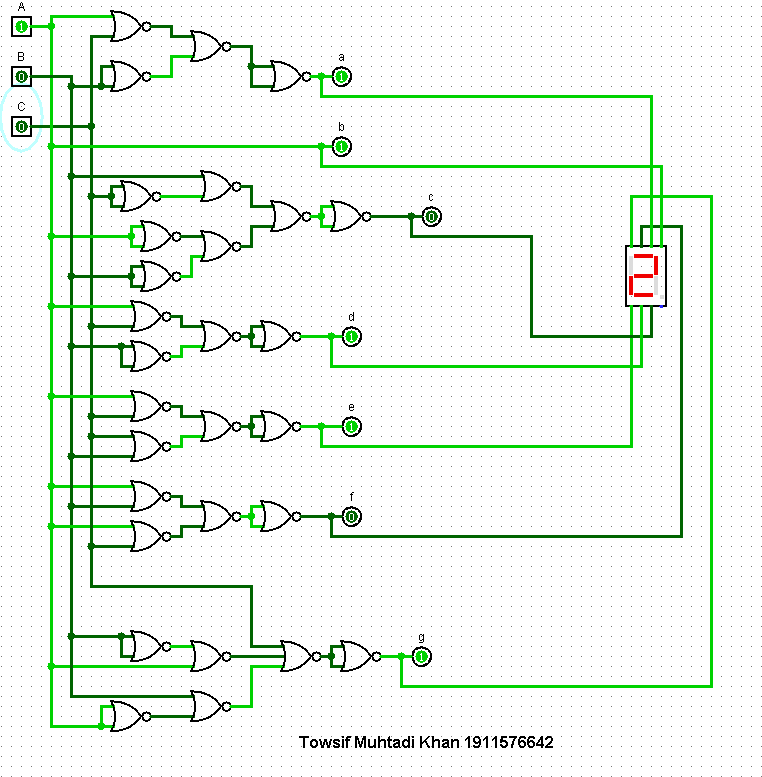
**a** = B’+A’C’, **b** = A, **c** = B’C+AB, **d** = B’+A’C’, **e** = A’C’ + B’C’

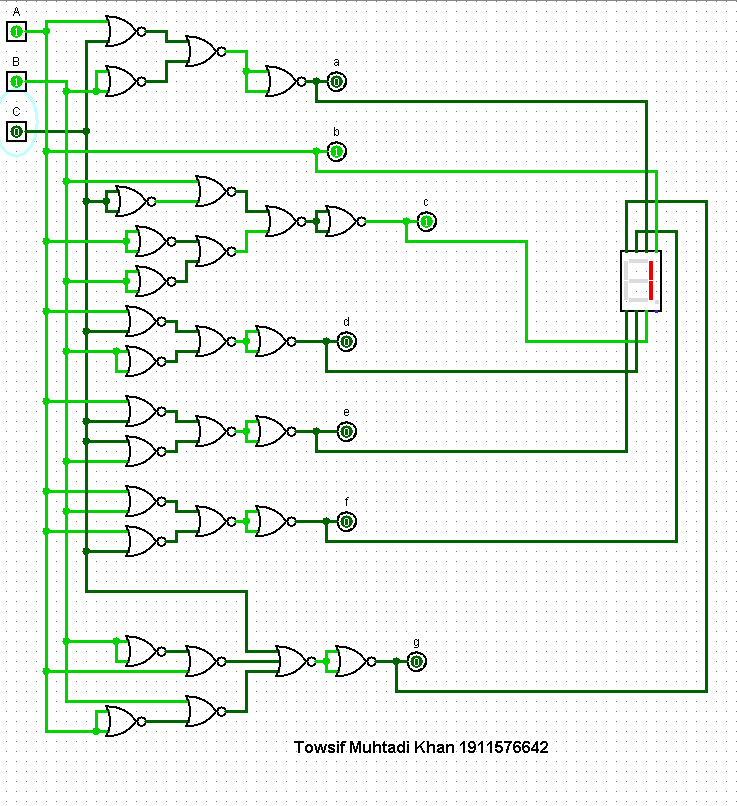
**f** = A’B’ + A’C’, **g** = C+A’B+AB’

The circuit diagram using NOR gates will be:

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**Figure:** *Circuit Diagram (Using NOR Gates)*